WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a state code register that stores a state code representing a present internal state;

a state transition logic unit configured to determine a state code for a next internal state to be transited in accordance with a predetermined logic, based on a state code provided from the state code register and an input command instructing transition to a required state, and to set the determined state code into the state code register with synchronizing an internal clock;

an expected value register configured to hold an internal state to be detected, as an expected value code; and

a comparing unit that compares the state code set in the state code register by the state transition logic unit to the expected value code in the expected value register and supplying an equal state signal when they coincide.

2. The semiconductor device according to claim 1, further comprising:

a timer unit configured to count a residence period at a present internal state with synchronizing to an internal clock;

wherein the state transition logic unit is further configured to input a count value from the timer unit so that it further determines a state code for a next internal state to be transited based on the count value provided from the timer.

3. The semiconductor device according to claim 2, wherein:

the timer unit stops or resets its counting operation by receiving the equal state signal from the comparing unit; and

the state transition logic unit stops a transition of an internal state based on the count value supplied from the timer unit.

4. The semiconductor device according to claim 1, further comprising:

an internal interrupt generating unit configured to generate and supply an internal interrupt command to the state transition logic unit by receiving the equal state signal provided from the comparing unit.

5. The semiconductor device according to claim 4, wherein:

the internal interrupt generating unit, is further configured to receive a test command for selecting either one of a normal mode or a test mode and an interrupt command indicating an interrupt operation externally, so that it provides the interrupt command during the normal mode and provides the internal interrupt command during the test mode to the state transition logic unit.

6. The semiconductor device according to claim 4, further comprising a unit configured to inform the equal state signal externally.

7. A method for checking a state transition of a semiconductor device, comprising:

determining a state code for a next internal state to be transited in accordance with a predetermined logic, based on a state code indicating a present internal state and a command instructing to transit to a required state;

setting the determined state code into a state code register, with synchronizing an internal clock;

setting an internal state to be detected into an expected value register as an expected value code;

comparing the state code set into the state code register with the expected value code set into the expected value register; and

outputting an equal state signal when the state code coincides with the expected value code.

8. The state transition checking method according to claim 7,further comprising determining the state code for a next internal state to be transited, based on a count value indicating a residence period at a present internal state.

9. The state transition checking method according to claim 7, further comprising prohibiting occurrence of a transition from a present internal state when the equal state signal is provided after the comparison, except transition to the predetermined internal state.

10. The state transition checking method according to claim 7, further comprising generating an internal interrupt command for transiting into a predetermined internal state when the equal state signal is supplied after the comparison.

11. The state transition checking method according to claim 7, further comprising utilizing the equal state signal after the comparison as an external trigger signal for evaluating or analyzing an internal state.

12. The state transition checking method according to claim 7, further comprising counting a residence period at a present internal state with synchronizing to an internal clock.

13. The state transition checking method according to claim 7, further comprising inputting a count value to further determine a state code for a next internal state to be transited.

14. The state transition checking method according to claim 7, further comprising stopping or resetting a counting operation by receiving the equal state signal.

15. The state transition checking method according to claim 7, further comprising stopping a transition of an internal state based on the count value supplied by a timer unit.

16. A semiconductor device, comprising:

a state code register that stores a state code representing a present internal state;

means for determining a state code for a next internal state to be transited in accordance with a predetermined logic, based on a state code provided from the state code register and an input command instructing transition to a required state, and setting the determined state code into the state code register with synchronizing an internal clock;

an expected value register configured to hold an internal state to be detected, as an expected value code; and

a comparing unit that compares the state code set in the state code register by the means for determining the expected value code in the expected value register and supplying an equal state signal when they coincide.

17. The semiconductor device according to claim 16, further comprising:

a timer unit configured to count a residence period at a present internal state with synchronizing to an internal clock;

wherein the means for determining further inputs a count value from the timer unit so that it further determines a state code for a next internal state to be transited based on the count value provided from the timer.

18. The semiconductor device according to claim 17, wherein:

the timer unit stops or resets its counting operation by receiving the equal state signal from the comparing unit; and

the means for determining stops a transition of an internal state based on the count value supplied from the timer unit.

19. The semiconductor device according to claim 16, further comprising:

an internal interrupt generating unit configured to generate and supply an internal interrupt command to the means for determining by receiving the equal state signal provided from the comparing unit.

20. The semiconductor device according to claim 19, further comprising a unit configured to inform the equal state signal externally.